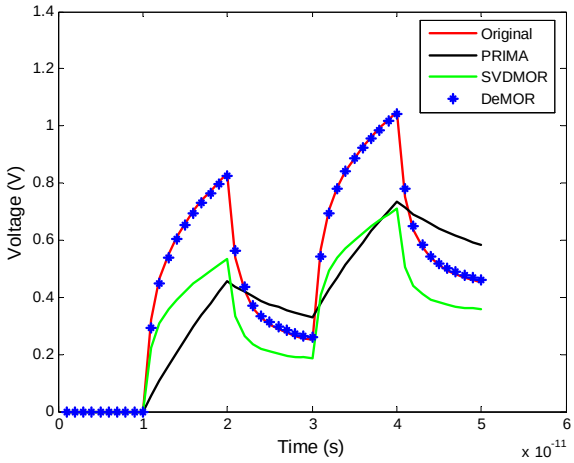
Integrated Circuit Complexity Reduction Tool

Integrated circuits in the nanometer range can have millions of parasitic RLC elements at the post layout stage, which renders the simulation of parasitic intensive post-layout VLSI circuits extremely difficult using today's simulation techniques.

Model order reduction (MOR) is one tool used to reduce the complexity of complex parasitic interconnect systems in VLSI while maintaining accuracy. Existing MOR schemes such as projection-based PRIMA can be used, but these schemes fall short in systems with massive numbers of outputs and inputs such as the bit and word lines in the memory circuits.

Researchers at the University of California have developed an innovative MOR scheme called "DeMor", which adopts a decentralized reduction strategy and allows the efficient reduction of circuits with many ports. For the first time, this new reduction technique overcomes the longstanding problem of reducing circuits with massive number of terminals and the reduction technique can reduce many practical industry circuits efficiently.

For example, in simulations with a 10,000 node system with 100 ports, UC's DeMor generated a 7^{th} order reduced model which predicted the original data very well, while tools such as PRIMA and SVDMOR using the same order resulted in very large errors.



This figure compares the performance of UC's DeMOR against PRIMA and SVDMOR in a simulated system having 10,000 nodes and 100 power sources using 7th order for the reduced models. The voltage at a single node in the system is simulated and the DeMOR scheme does a superior job of predicting voltage at this node.